OFE TARES

Signature

12/2/05

Date

PTO/SB/21 (04-04)

PTO/SB/21 (04-04)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

атна					
TRANSMITTAL			Application Number	10/796727	
		F	Filing Date	3/9/2004	
F	ORM	F	First Named Inventor	Byers et al.	
(to be used for all con	respondence after initi	al filing)	Art Unit		
		T E	Examiner Name		
Total Number of Pages	in This Submission		Attorney Docket Number	MP0787	
		ENCLOSI	JRES (check all that apply)		
Fee Transmittal Fo	orm	Drawing(s	s)	After Allowance Technology Cer	Communication to nter (TC)
· Fee Attached		Licensing	-related Papers	Appeal Commu	nication to Board of terferences
Amendment / Repl	у	Petition		Appeal Commu	nication to TC Brief, Reply Brief)
After Final			Convert to a al Application	Proprietary Information	
Affidavits/decla			Attorney, Revocation of Correspondence Address	Status Letter	
Extension of Time Request		Terminal	Disclaimer	Other Enclosur	e(s) alow):
Express Abandonn	nent Request		or Refund ber of CD(s)	Statement Under 37 CFR 3.73(b), Change of Power of Attorney, Change of Correspondence Address, and	
☐ Information Disclos	sure Statement			Copy of Assi	ttorney Docket Nunber; gnment from Qlogic to Marvell International card
Certified Copy of P Document(s)	Priority	Remarks	fees that may be requ	hereby authorized to c irred under 37 CFR 1.1 . A duplicate copy of the	16 or 1.17 to Deposit
Response to Missin	Response to Missing Parts/ Incomplete Application			The second secon	S. Is onologo.
Response to M Parts under 37 1.52 or 1.53					
	SIGNA	TURE OF AP	PLICANT, ATTORNEY, C	R AGENT	
Firm or Individual name	Harness, Dickey &		Attorney Name Donald J. Daley	Reg. No. 34,313	
		1	<del>'</del>		<del></del>



#### **PATENT**

#### IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.:

10/796,727

Filing Date:

3/9/2004

Applicant:

Byers et al.

Title:

Servo Controller Interface Module For Embedded

**Disk Controllers** 

Old Attorney Docket: QE1056.US

New Attorney Docket: MP0787

Director of the United States Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450

# STATEMENT UNDER 37 CFR 3.73(b), CHANGE OF POWER OF ATTORNEY, CHANGE OF CORRESPONDENCE ADDRESS, AND CHANGE OF ATTORNEY DOCKET NUMBER.

#### 1. STATEMENT UNDER 37 CFR 3.73(b).

Under 37 C.F.R. § 3.73(b), the undersigned hereby states that the below-named Assignee is an assignee in the above-identified Application:

Assignee:

Marvell International Ltd.

Argyle House 41A Cedar Avenue

Hamilton, HM12, Bermuda

The documentary evidence of a chain of title from the original owner to the Assignee is provided in the Assignment Document(s):

From: Byers et al.

To: QLOGIC CORPORATION
Reel No. 016437 Frame No. 0862.

From: QLOGIC CORPORATION

To: MARVELL INTERNATIONAL LTD.

Filed herewith.

Page 1 of 2

# 2. REVOCATION OF PRIOR POWERS OF ATTORNEY.

I hereby revoke all prior powers of attorney in this application.

# 3. APPOINTMENT OF NEW POWER OF ATTORNEY

I hereby appoint each practitioner at Customer No. **26703** my attorney with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith.

# 4. CHANGE OF CORRESPONDENCE ADDRESS

I request the Patent and Trademark Office to direct all correspondence and telephone calls relative to this application to:

Harness, Dickey & Pierce, PLC.
P.O. Box 828, Bloomfield Hills, Michigan 48303
Telephone: (248) 641-1600
Fax: (248) 641-0270

### 5. CHANGE OF ATTORNEY DOCKET NUMBER

I hereby request the Patent and Trademark Office to change the attorney docket number to MP0787.

The undersigned, whose title is supplied below, is empowered to sign this certificate on behalf of the assignee.

Date: NOV 2 4 2005

Signature: \_

Name: (Print) CAROL FEATHERS

Title: (Print) General Manager

Page 2 of 2

10/796,727



#### **United States Patent and Trademark Office**

Home | Site Index | Search | Guides | Contacts | eBusiness | eBiz alerts | News | Help



### Assignments on the Web > Patent Query

# Patent Assignment Abstract of Title NOTE:Results display only for issued patents and published applications. For pending or abandoned applications please consult USPTO staff.

**Total Assignments: 1** 

Patent #: NONE Issue Dt: Application #: 10796727 Filing Dt: 03/09/2004

Publication #: US20040193743 Pub Dt: 09/30/2004

Inventors: Larry L. Byers, David M. Purdham, Michael R. Spaur

Title: Servo controller interface module for embedded disk controllers

Assignment: 1

Conveyance: ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS).

Assignors: PURDHAM, DAVID M. Exec Dt: 08/23/2005

SPAUR, MICHAEL R. Exec Dt: 08/23/2005

BYERS, LARRY L.

Assignee: QLOGIC CORPORATION

26650 ALISO VIEJO PARKWAY ALISO VIEJO, CALIFORNIA 92656

Correspondent: TJ SINGH

2 PARK PLAZA, SUITE 510

IRVINE, CA 92614

Search Results as of: 12/01/2005 02:50 PI

Exec Dt: 08/23/2005

If you have any comments or questions concerning the data displayed, contact OPR / Assignments at 571-272-3350

| .HOME | INDEX| SEARCH | eBUSINESS | CONTACT US | PRIVACY STATEMENT

#### **ASSIGNMENT**

For valuable consideration, QLOGIC CORPORATION, a Delaware corporation having place of business at 26650 Aliso Viejo Parkway, Aliso Viejo, California, 92656 ("Assignor") hereby assigns to MARVELL INTERNATIONAL LTD., a corporation organized under the laws of Bermuda and having its registered office at Canon's Court, 22 Victoria Street, Hamilton HM 12, Bermuda ("Assignee"), the entire right, title and interest throughout the world in the inventions and improvements which are the subject of patents or applications for patent listed in Attachment A, this assignment including said patents and applications for patent, any and all United States and foreign patents, utility models, and design registrations granted for any of said inventions or improvements, any reexaminations, extensions, reissues, continuations, and divisions of said patents and applications for patent, any foreign patent applications related to said patents and applications for patent, and the right to claim priority based on the filing date of said patents or applications for patent under the International Convention for the Protection of Industrial Property, the Patent Cooperation Treaty, the European Patent Convention, and all other treaties of like purposes; Assignor authorizes the Assignee to apply in all countries in the name of the inventors or in its own name for patents, utility models, design registrations and like rights of exclusion and for inventors' certificates for said inventions and improvements; and Assignor agrees for itself, its heirs, legal representatives and assigns, without further compensation to perform such lawful acts and to sign such further applications, assignments, preliminary statements and other lawful documents as the Assignee may reasonably request to effectuate fully this assignment.

> QLOGIC CORPORATION, a Delaware corporation

Anthony J. Massetti Senior Vice President and

Chief Financial Officer

November 4, 2005

## Attachment A

Country	Title	Serial No.	Filing Date	Patent No.	Issue Date
USA	Cylinder Defect Management System For Data Storage	07/285,808	12/16/1988	4935825	7/19/1990
USA	Buffer Memory Data Flow Controller	08/020,058	2/19/1993	5249271	9/28/1993
USA	Method And Apparatus To Determine The Log Of An Element In Gf(2m) With The Help Of A Small Adjustable Size Table	07/736461	7/26/1991	5313474	5/17/1994
USA	Method And Apparatus For Initializing An ECC Circuit	07/974,158	11/10/1992	5428627	6/27/1995
USA	System And Method For Generating Unique Sector Identifiers For An Identificationless Disk Format	08/372,072	1/12/1995	5627695	5/6/1997
USA	Circuit And Method For Rapid Checking Of Error Correction Codes Using Cyclic Redundancy Check	09/096,709	6/12/1998	6092231	7/18/2000
CA	Circuit And Method For Rapid Checking Of Error Correction Codes Using Cyclic Redundancy Check	2333386	5/27/1999		
EP	Circuit And Method For Rapid Checking Of Error Correction Codes Using Cyclic Redundancy Check	925959	5/27/1999	1090462 B1	8/3/2005
JP	Circuit And Method For Rapid Checking Of Error Correction Codes Using Cyclic Redundancy Check	2000- 551486	5/27/1999		

Country	Title	Serial No.	Filing Date	Patent No.	Issue Date
USA	Systems And Methods For A Disk Controller Memory Architecture	09/547,567	4/12/2000	6330626	12/11/2001
USA	Method For Context Switching With A Disk Controller	09/548,330	4/12/2000	6401149	6/4/2002
CA	Systems And Methods For A Disk Controller Memory Architecture	2370596	5/5/2000		
EP	Systems And Methods For A Disk Controller Memory Architecture	930436	5/5/2000		
JP	Systems And Methods For A Disk Controller Memory Architecture	2000615882	5/5/2000		
KR	Systems And Methods For A Disk Controller Memory Architecture	102001- 7014078			
PCT	Systems And Methods For A Disk Controller Memory Architecture	PCTUS0012 433	5/5/2000		
USA	Circuit And Method For Monitoring Sector Transfers To And From Storage Medium	09/243,295	2/2/1999	6487631	11/26/2002
USA	Disk Drive Controller Circuit And Method For Skipping Defective And/Or Undesired Sectors	09/326,851	6/7/1999	6470461	10/22/2002
CA	Disk Drive Controller Circuit And Method For Skipping Defective And/Or Undesired Sectors	2375672	6/1/2000		
EP	Disk Drive Controller Circuit And Method For Skipping Defective And/Or Undesired Sectors	941177	6/1/2000		
JP	Disk Drive Controller Circuit And Method For Skipping Defective And/Or Undesired Sectors	2001502120	6/1/2000		

Country	Title	Serial No.	Filing Date	Patent No.	Issue Date
KR	Disk Drive Controller Circuit And Method For Skipping Defective And/Or Undesired Sectors	102001- 7015758			
PCT	Disk Drive Controller Circuit And Method For Skipping Defective And/Or Undesired Sectors	PCTUS0015 084	6/1/2000		
USA	Methods And Systems For Arbitrating Access To A Disk Controller Buffer Memory By Allocating Various Amounts Of Times To Different Accessing Units	09/275,629	3/24/1999	6530000	3/4/2003
CA	Arbitration Methods And Systems For Arbitrating Access To A Disk Controller Memory	2364625	3/23/2000		
EP	Arbitration Methods And Systems For Arbitrating Access To A Disk Controller Memory	918322			
JР	Arbitration Methods And Systems For Arbitrating Access To A Disk Controller Memory	2000607076	3/23/2000		
KR	Arbitration Methods And Systems For Arbitrating Access To A Disk Controller Memory	102001- 7012114			
PCT	Arbitration Methods And Systems For Arbitrating Access To A Disk Controller Memory	PCTUS0007 780	3/23/2000		
USA	Disk Controller Configured To Perform Out Of Order Execution Of Write Operations	09/643,636	8/22/2000	6826650	11/30/2004
USA	Disk Controller Configured To Perform Out Of Order Execution Of Write Operations	10/920,881	8/18/2004		

Country	Title	Serial No.	Filing Date	Patent No.	Issue Date
EP	Disk Controller Configured To Perform Out Of Order Execution of Write Operations	958970	7/17/2001		
JP	Disk Controller Configured To Perform Out Of Order Execution Of Write Operations	2002521285	7/17/2001		
KR	Disk Controller Configured To Perform Out Of Order Execution Of Write Operations	10-2003- 7002436			
PCT	Disk Controller Configured To Perform Out Of Order Execution of Write Operations	PCTUS0122 404	7/17/2001		
USA	Controller For A Disk Drive And Method For Writing Onto And Reading From A Disk	09/049,157	3/26/1998		
PCT	Controller For A Disk Drive And Method For Writing Onto And Reading From A Disk	PCTUS9906 635	3/26/1999		
USA	Circuit And Method For Rapid Checking Of Error Correction Codes Using Cyclic Redundancy Check	09/085,765	5/27/1998		
PCT	Circuit And Method For Rapid Checking Of Error Correction Codes Using Cyclic Redundancy Check	PCTUS9911 819	5/27/1999		
USA	System And Method For In-Line Error Correction For Storage Systems	10/199,911	7/19/2002	6961877	Nov-01, 2005
USA	Method And System For Using An Interrupt Controller In An Embedded Disk Controller	10/384,991	3/10/2003		

Country	Title	Serial No.	Filing Date	Patent No.	Issue Date
USA	Method And System For Automatic Time Base Adjustment For Disk Drive Servo Controllers	10/384,992	3/10/2003		
USA	Method And System For Embedded Disk Controllers	10/385,022	3/10/2003		
USA	Method And System For Supporting External Serial Port Devices Using A Serial Port Controller In Embedded Disk Controllers	10/385,039	3/10/2003		
USA	Method And System For Monitoring Embedded Disk Controller Components	10/385,042	3/10/2003		
USA	Method And System For Using An External Bus Controller In Embedded Disk Controllers	10/385,056	3/10/2003		
USA	Method And System For Collecting Servo Field Data From Programmable Devices In Embedded Disk Controllers	10/385,405	3/10/2003		
USA	System And Method For Performing Parity Checks In Disk Storage Systems	10/429,495	5/5/2003		
USA	System And Method For Transferring Data In Storage Controllers	10/619,954	7/15/2003		
USA	System And Method For Using Tap Controllers	10/686,151	10/15/2003		
USA	System And Method For Concatenating Data	10/761,786	1/21/2004		

Country	Title	Serial No.	Filing Date	Patent No.	Issue Date
JSA	Method And System For Head Position Control In Embedded Disk Drive Controllers	10/793,207	3/4/2004		
JSA	Servo Controller Interface Module For Embedded Disk Controllers	10/796,727	3/9/2004		
USA	Integrated Memory Controller	10/867,113	6/14/2004		
USA	System And Method For Reading And Writing Data Using Storage Controllers	10/878,803	6/28/2004		
USA	System And Method For Transferring Data Using Storage Controllers	10/893,822	7/19/2004		
USA	System And Method For Transmitting Data In Storage Controllers	10/894,143	7/19/2004		
USÁ	Dynamic WWN Storage Module For Storage Controllers	10/894,144	7/19/2004		
USA	System And Method For Controlling Buffer Memory Overflow And Underflow In Storage Controllers	10/894,208	7/19/2004		
USA	Power Save Module For Storage Controllers	10/965,468	10/13/2004		
USA	System And Method For Conducting BIST Operations	10/983,944	11/8/2004		
USA	Method And System For Processing Frames In Storage Controllers	10/989,060	11/15/2004		
USA	Method And System For Performing CRC	11/056,320	2/11/2005		

Country	Title	Serial No.	Filing Date	Patent No.	Issue Date
USA	Method And System For Read Gate Timing Control For Storage Controllers	11/099,746	4/6/2005		
PCT	Method And System Embedded Disk Controllers	PCTUS0407 119	3/9/2004		